HDG205-WiFi 802.11n/g/b System in Package

Data Sheet

HDG205

WiFi SIP component

H&D Wireless

Revision History

Revision	Revision date	Description
PA1	2015-01-29	First issue
PA2	2015-03-11	Updated order information

1 INTRODUCTION

1.1 Overview

HDG205 is a complete WLAN System In Package, SIP, solution specifically designed to address the proliferation of Wi-Fi technology into embedded devices.
HDG205 enables a cost efficient ultra low power, high performance and feature rich client solution. It provides up to 65 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.
HDG205 integrates RF, baseband/MAC, memory, RF filters and oscillator into a highly integrated and optimized SIP (System In Package) solution with high quality and reliability. This minimizes the need of external components, simplifying assembly and test.
This highly integrated solution is optimized for customer applications running on a host CPU.
The host interface supports SDIO and SPI. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces.
MAC address, firmware and calibration data are stored in the on board memory.

1.2 Key Features

- Support for 802.11b/g/n
- Data Rates: 1, 2, 5.5, 6, 7.2, 9, 11, 12, 14.4, 18, 21.7, 24, 28.9, 36, 43.3, 48, 54, 57.8, 65 Mbps
- Modulation: QPSK, 16QAM, 64QAM DBPSK, DQPSK, CCK, OFDM with BPSK
- Open WEP, WPA/WPA2 encryption
- No external RF components
- Low power consumption due to efficient PA design
- LDO:s for RF-VCO and crystal oscillator for lower pushing
- An internal 32 kHz oscillator maintains real time in power save mode, allows the high frequency clock to be turned off.
- Support for an external 32kHz real time clock
- Extensive DMA hardware support for data flow to reduce CPU load.
- Advanced power management for optimum power consumption at varying load.
- External interfaces SDIO/SPI
- On-board High Frequency High Precision Oscillator 40 MHz
- Wide Range Supply Voltage, 2.85-4.35 V
- Small footprint 8 x 8 mm (64 mm2) 44-pin QFN
- RoHS Compliant

2 HARDWARE ARCHITECTURE

2.1 Block Diagram

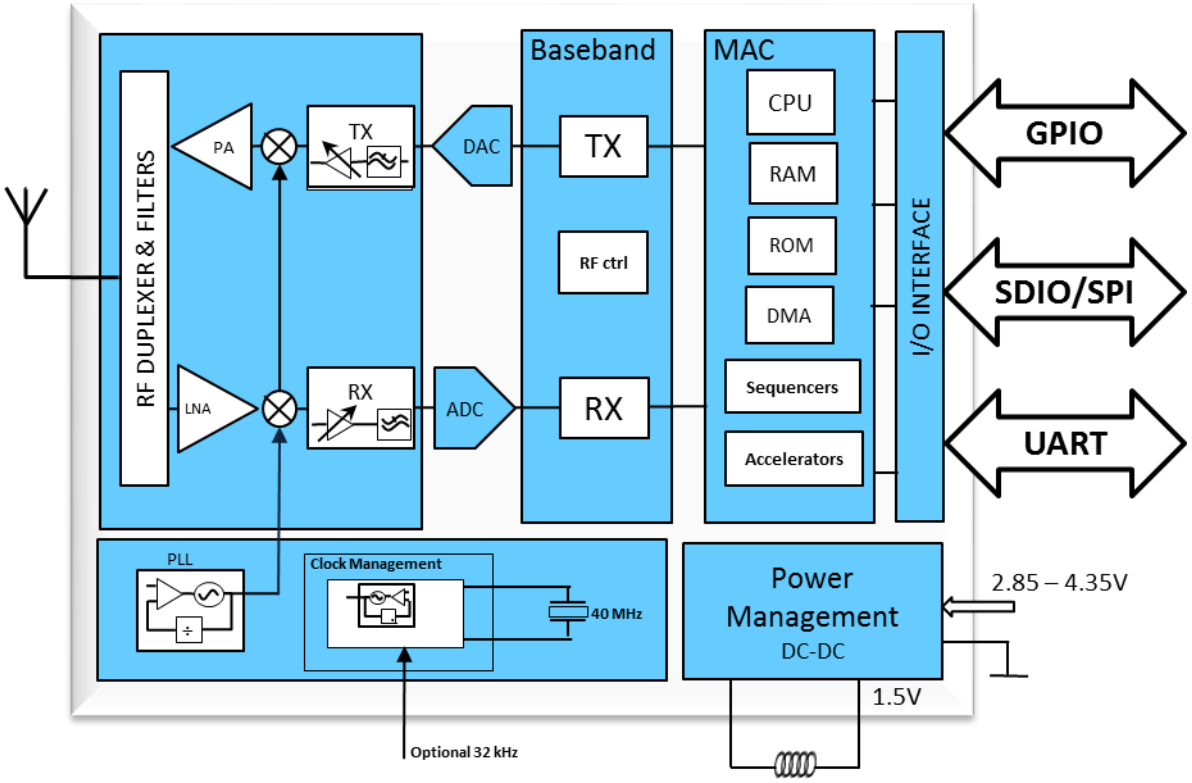

Figure 2-1: Block Diagram

2.2 Order information

Part No.	Temperature Range	Package	Shipment package
HDG205-DC-N2	Commercial (0 to 70°C)	QFN 44+4 pins,8x8 mm	Tape & Reel
HDG205-DC-N3	Commercial (0 to 70°C)	QFN 44+4 pins,8x8 mm	Tray
HDG205-DM-N2	Industrial (-20 to 85°C)	QFN 44+4 pins,8x8 mm	Tape & Reel
HDG205-DM-N3	Industrial (-20 to 85°C)	QFN 44+4 pins,8x8 mm	Tray

Table 2-1: Order Information

3 ELECTRICAL DATA

3.1 Absolute maximum ratings

Rating	Min	Max	Unit
Supply voltage	-0.3	4.55	V
Supply voltage I/O	-0.3	3.65V and VBAT + 0.3[1]	V
Input RF level		10	dBm
Storage temperature	-50	+125	°C
Lead temperature (No Pb), solder 40sek*) ***Ref. IPC/JEDEC J-STD-020C, July 2004**		+260	°C

Table 3-1: Absolute maximum ratings. Exceeding any of the maximum ratings, even briefly lead to deterioration in performance or even destruction. Values indicates condition applied one at the time.

1: Note that during power on/off ramping supply voltage I/O must not exceed VBAT with more than 0.3V

3.2 Electro Static Discharge (ESD)

HDG205 withstands ESD voltages up to 2000V HBM (Human Body Model) according to JESD22-A114 and up to 300 V CDV (Charged Device Model) according to JESD22-A115.

3.3 Recommended operating conditions

Rating	Min	Typ	Max	Unit
Supply Voltage VBAT	2.85	3.6	4.35	V
Supply Voltage VDD_IO	1.62	3.6	3.6 or VCC+0.3	V
Supply Voltage IO with VBAT 0V		0	0.2	V
VDD_DCDC		1.5		V
Operating temperature (Commercial grade)	0	+25	+70	°C
Operating temperature (Industrial grade)	-20	+25	+85	°C

Table 3-2: Recommended operating conditions

3.4 Power Consumption

Conditions: Tamb = 25 °C, VBAT=3.6V, Internal DC-DC for 1.2V

Mode	Conditions	Min	Typ.	Max	Unit
TX 802.11 b	CCK 11Mbps, Pout=18 dBm		205	230	mA
TX 802.11 g	OFDM 54 Mbps, Pout=15 dBm		165	200	mA
TX 802.11 n	OFDM 65 Mbps, Pout=14 dBm		140	170	mA
RX 802.11 b	Normal mode – Max Sensitivity		53	59	mA
RX 802.11 g	Normal mode – Max Sensitivity		56	64	mA
RX 802.11 n	Normal mode – Max Sensitivity		56	64	mA
Sleep	Power Save active. Between beacon listening		80		µA
Power Save	DTIM = 1, Beacon Interval 100ms		2.7		mA
Power Save	DTIM = 3, Beacon Interval 300ms		1.3		mA
Shutdown	SHUTDOWN held low		12		µA

Table 3-3: Typical current consumption in different modes.

3.5 RF Performance

Conditions: VBAT= 3.6V, T_{amb}= 25°C Spectrum Mask and BER according to IEEE 802.11b/g/n specification.

Parameter	Conditions	Min	Typical	Max	Units
Frequency range		2412		2472	MHz
Supported Channels		Ch.1 (2412 MHz)		Ch. 13 (2472 MHz)	
RF impedance			50		ohm
Transmitter performance[1]					
Output power	QPSK, Calibrated.	+16	+17	+18	dBm
Output power	OFDM 54 Mbit/s, Calibrated.	+13	+14	+15	dBm
Output power	HT20 MSC6, Calibrated.	+10	+11	+12	dBm
EVM at +18dBm	CCK, ch. 1- ch. 13		14		%
EVM at +15dBm	OFDM 802.11b/g		5.0		%
EVM at +14dBm	OFDM 802.11n (MSC7)		4.0		%
Receiver performance 11b/g					
Receiver sensitivity	DPSK 1Mbit/s		-94	-87	dBm
Receiver sensitivity	QDPSK 2Mbit/s		-91	-85	dBm

Receiver sensitivity	CCK/DPSK 5.5Mbit/s		-89	-84	dBm
Receiver sensitivity	CCK/BPSK 11Mbit/s		-86	-81	dBm
Receiver sensitivity	OFDM/BPSK 6Mbit/s		-89	-84	dBm
Receiver sensitivity	OFDM/BPSK 9Mbit/s		-88	-83	dBm
Receiver sensitivity	OFDM/QPSK 12Mbit/s		-86	-81	dBm
Receiver sensitivity	OFDM/QPSK 18Mbit/s		-84	-79	dBm
Receiver sensitivity	OFDM/16-QAM 24Mbit/s		-82	-76	dBm
Receiver sensitivity	OFDM/16-QAM 36Mbit/s		-79	-72	dBm
Receiver sensitivity	OFDM/64-QAM 48Mbit/s		-74	-68	dBm
Receiver sensitivity	OFDM/64-QAM 54Mbit/s		-72	-67	dBm
Receiver performance 11n					
Receiver sensitivity	MCS-0, OFDM/BPSK 7.2Mbit/s		-90	-83	dBm
Receiver sensitivity	MCS-1, OFDM/BPSK 14.4Mbit/s		-88	-80	dBm
Receiver sensitivity	MCS-2, OFDM/BPSK 21.7Mbit/s		-86	-78	dBm
Receiver sensitivity	MCS-3, OFDM/16-QAM 28.9Mbit/s		-83	-75	dBm
Receiver sensitivity	MCS-4, OFDM/16-QAM 43.4Mbit/s		-79	-71	dBm
Receiver sensitivity	MCS-5, OFDM/64-QAM 57.8Mbit/s		-72	-67	dBm
Receiver sensitivity	MCS-6, OFDM/64-QAM 65Mbit/s		-70	-66	dBm

Table 3-4: Receiver Performance

1. TX output power varies with temperature as shown in Figure 3-1

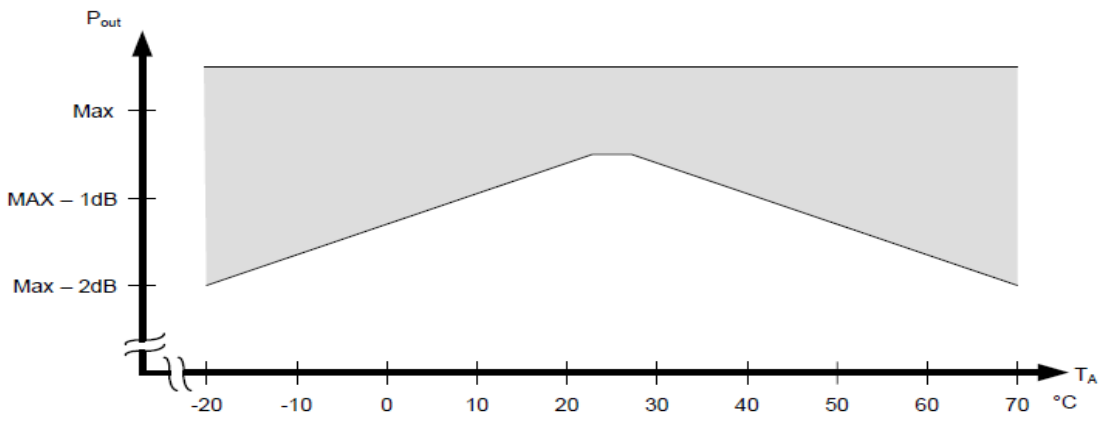

Figure 3-1: Pout vs. ambient temperature

2. TX Output power varies with temperature as shown in Figure 2

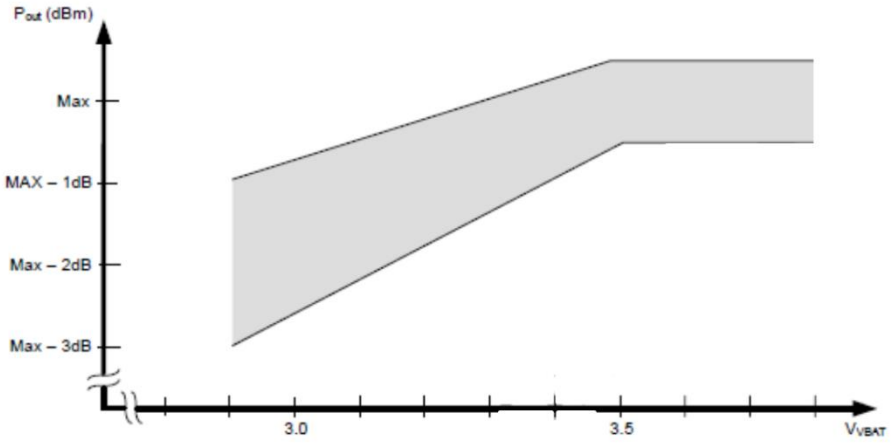

Figure 2: Output Power vs. VDD voltage

3.6 Digital pin characteristics

3.6.1 SDIO timing characteristics

The SDIO/SPI-interface can run in three different modes, SDIO 1-bit mode, SDIO 4-bit mode or in SDIO/SPI 1-bit mode. Timing can be set for Default speed mode or High speed mode.

SDIO 1-bit Default speed mode is selected at Power On Reset. The host can change mode by sending the corresponding command over the SDIO-interface.

The Default mode is showed in Figure 3-3 and Table 3-5. For the high speed mode see Figure 3-4 and Table 3-6

Condition: VDDIO_SDIO= 1.7 – 3.6 V, Tamb= 0 to +70°C

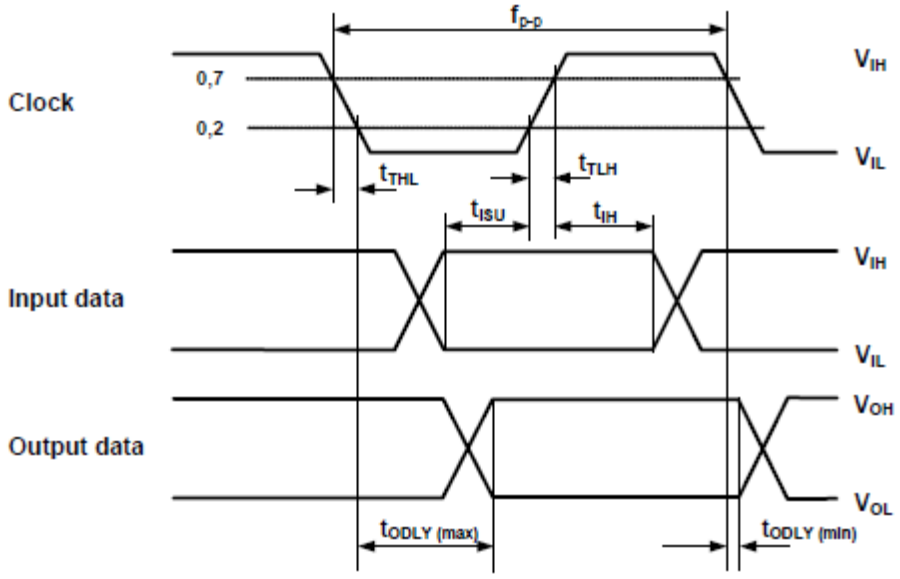

Figure 3-3: SDIO/SPI timing diagram (default mode

Parameter	Symbol	Min	Max	ns	Comments
Input set-up time	tISU	5		ns	
Input hold time	tIH	5		ns	
Clock fall time	tTHL		10	ns	
Clock rise time	tTLH		10	ns	
Output delay time	tODLY	0	14	ns	
Clock Frequency			25	MHz	

Table 3-5: SDIO timing parameter values (default mode)

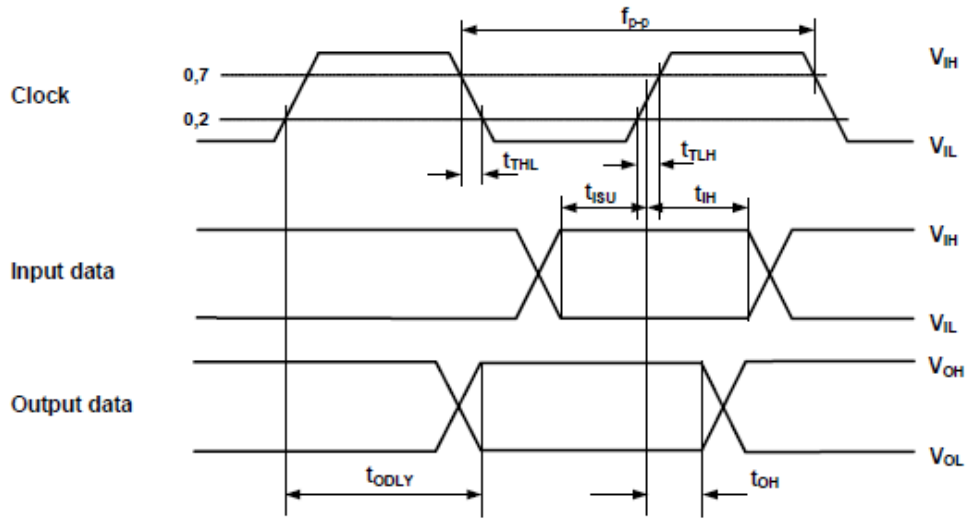

Figure 3-4: SDIO timing diagram (high speed mode)

Parameter	Symbol	Min	Max	ns	Comments
Input set-up time	tISU	6		ns	
Input hold time	tIH	2		ns	
Clock fall time	tTHL		3	ns	
Clock rise time	tTLH		3	ns	
Output delay time	tODLY	2,5	14	ns	
Output hold time	tOH	2.5		ns	
Clock Frequency			50	MHz	Decreasing to 33 MHz @1.7V

Table 3-6: SDIO timing parameter values (high speed mode)

3.6.2 Digital input/output pad (I/O)

The digital I/O pads are of type none inverting three-state driver/receiver. The I/O pin functional schematic is shown in Figure 3-5. It includes an input buffer and an output buffer with enable/disable control inputs. It also includes a hold-function. When an I/O is neither driven by the internal nor by an external circuitry, the hold function maintain the latest state of the I/O. This is the case for example when SHUTDOWN is active.

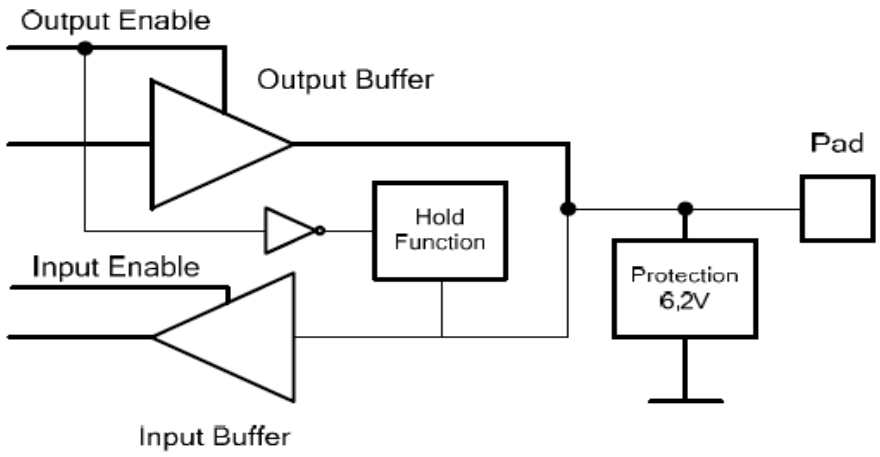

Figure 3-5: Function schematics of the I/O input pad configuration.

Parameter	Symbol	Min	Typ	Max	Units	Comments
Input low voltage	vIL	-0.3		0.25*V_{IO}	V	
Input high voltage	vIH	0.625*V_{IO}		V_{IO}+0.3	V	
Input leakage current	iIL	-1		1	µA	
Output low voltage	vOL			0.125*V_{IO}	V	I_{out}<1mA
Output high voltage	vOH	0.75*V_{IO}			V	I_{out}>-1mA
Input pin capacitance	cIP		2.5		pF	
VDDIO, VDD_SDIO	vIO	1.7		3.6	V	

Table 3-7: I/O pin DC characteristics.

3.6.3 Protection of digital pins

All digital pins are protected against over-voltage with a “snap-back” circuit connected between the pad and GND. The “snap-back” voltage is 6.2 V and the holding voltage is 6 V. This provides a satisfying protection against over voltages and ESD. Also there is a diode included to protect against reversed voltages.

3.6.4 Shutdown

The Shutdown input has a high impedance pull down resistor. Set the pin low or open to put HDG205 in shutdown mode. Pull the pin high to start HDG205. If a pull up resistor is used, recommended max value is 1Mohmand a decoupling capacitor of 0.1uF to ground.

Parameter	Symbol	Min	Typ	Max	Units	Comments
Input low voltage	vIL	-0.3		0.2	V	
Input high voltage	vIH	1.65		VBAT+0.3	V	
Input leakage current	ıIL	-1		+2	µA	
Pull down resistance	ıIN		2		Ohm	

Table 3.11: SHUTDOWN pin DC characteristics.

4 PIN CONFIGURATIONS

4.1 Pin Configuration

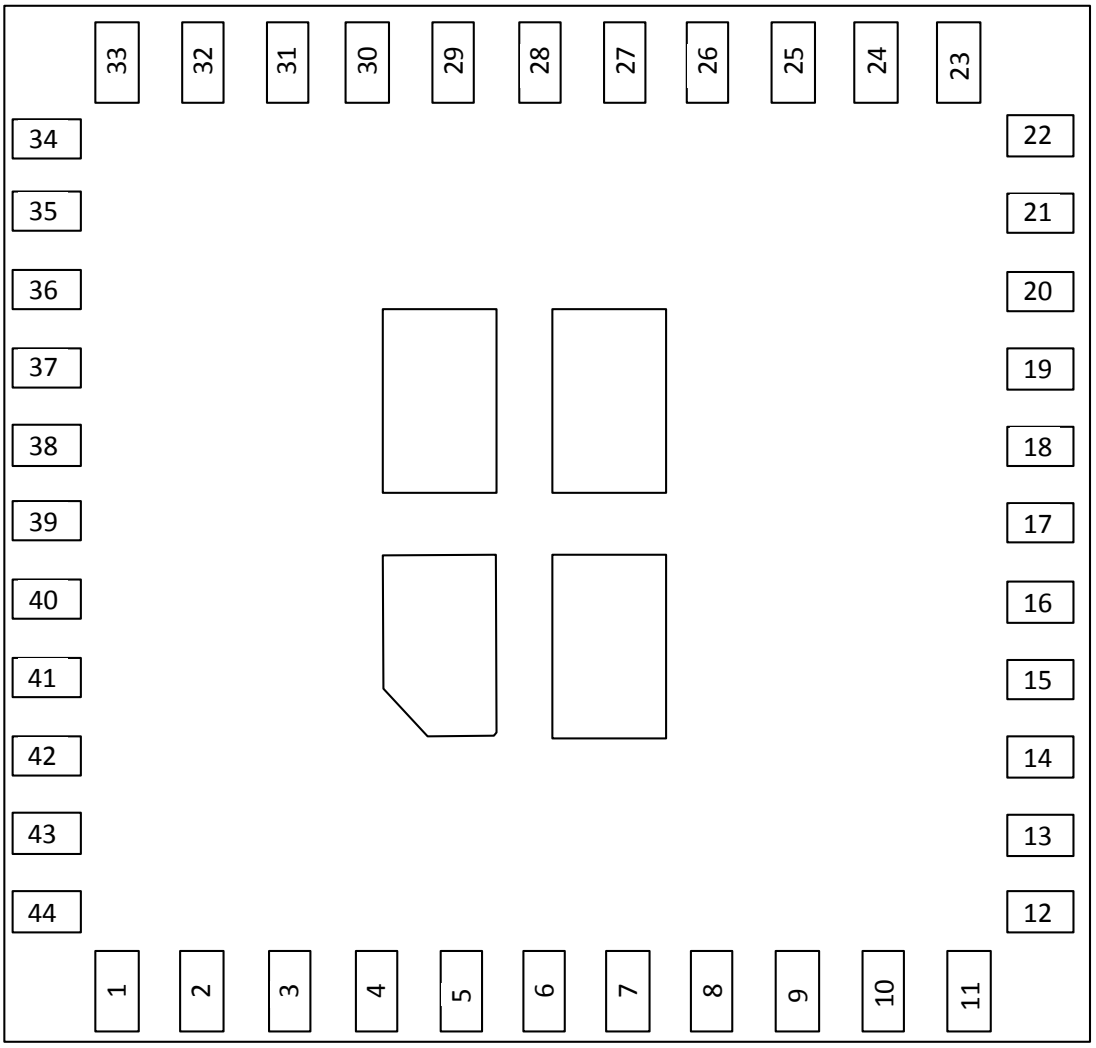

Figure 4.1: Package pin out. Top view 44 pin QFN

4.2 Pin assignments

Pin	Pin Name	Type	IO Supply Domain	Description		Pin state when SHUTDOWN is low
				UART mode	SPI Mode	
1	SPI_CLK	I	VDD_SPI	No Connection	SPI CLK	Tri State
2	UART_RX/SPI_MISO	O	VDD_SPI	UART_RX	SPI MISO	Tri State
3	UART_CTS/SPI_IRQ	I/O	VDD_SPI	UART_CTS	SPI IRQ	Tri State
4	GND	S	VDD	Ground		-
5	ANT	RF	-	Antenna Port (50 Ohm) for WLAN		OFF floating
6	GND	S	All	Ground		-
7	ICE_TDI	IPU	VDD_SPI	ICE Test Data Input, do not connect		Tri State
8	GPIO1	O	VDD_IO	General purpose IO defined by FW		Tri State
9	ICE_TCK	IPU	VDD_SPI	ICE Test Clock, do not connect		Tri State
10	NO CONNECTION	-	-	Do not connect		-
11	ICE_TMS	IPU	VDD_SPI	ICE Test Mode Select, do not connect		Tri State
12	NO CONNECTION	-	-	Do not connect		-
13	ICE_TDO	I/O	VDD_SPI	ICE Test Data output, do not connect		Tri State
14	GPIO2	O	VDD_IO	General purpose IO defined by FW		Tri State
15	GPIO3	I/O	VDD_IO	General purpose IO defined by FW		Tri State
16	GPIO4	I/O	VDD_IO	General purpose IO defined by FW		Tri State
17	GPIO5	I/O	VDD_IO	General purpose IO defined by FW		Tri State
18	VDD_DCDC	S	VDD	Internally Generated digital VDD 1.5V, de-couple with a 1uF capacitor to GND		Off
19	UARTb_SPI/WAKE_UP	I	VDD_IO	Host interface select, internal pull-up Initially Low=UART Host interface select Initially High= SPI Slave Thereafter HDG820 WAKE_UP		Tri State
20	VDD_LDO_IO	S	VDD	IO supply voltage. De-couple with 0.1uF to GND		Off
21	VDD	S	VDD	Supply voltage, de-couple with a 1uF capacitor to GND		On
22	GPIO6	I/O	VDD_IO	General purpose IO defined by FW		Tri State
23	GND	S	All	Ground		
24	SHUTDOWN	A1		Reset pin. Active Low		Low
25	VDD_DCDC	S	VDD	DIGITAL VDD 1.5V, de-couple with a 1uF capacitor to GND close to package pin		Off
26	DCDC_OUT	O	VDD	DCDC Output connect via 3.3uH to VDD_DCDC Close to package pin		Off

27	VDD	S	VDD	Supply voltage, Decouple with 0.1uF to GND		On
28	NO CONNECTION	-	-	Do not connect		-
29	NO CONNECTION	-	-	Do not connect		-
30	NO CONNECTION	-	-	Do not connect		-
31	GND	S	All	GND		-
32	NO CONNECTION	-	-	Do not connect		-
33	NO CONNECTION	-	-	Do not connect		-
34	NO CONNECTION	-	-	Do not connect		-
35	NO CONNECTION	-	-	Do not connect		-
36	NO CONNECTION	-	-	Do not connect		-
37	LED1	I/O	VDD_IO	LED signal active high. Indicates WLAN association[1]		Tri state
38	VDD_IO	S	VDD_IO	VDD_IO Supply for digital I/Os except SPI domain		On
39	HOST_ATT	O	VDD_IO	Host wake-up pin		Tri state
40	UART_TX/SPI_CS	I/O	VDD_SPI	UART_TX	SPI CS active low	Tri state
41	SPI_MOSI	I/O	VDD_SPI	No Connection	SPI MOSI	Tri state
42	NO CONNECTION	-	-	Do not connect		-
43	VDD_SPI	S	VDD_SPI	Host interface I/O Supply, decouple with 0.1uF to GND		On
44	UART_RTS	I/O	VDD_SPI	UART_RTS	No Connection	Tri state
45	GND	S	All	Ground		-
45	GND	S	All	Ground		-
45	GND	S	All	Ground		-
45	GND	S	All	Ground		-

Table 4.1: Pin Description for the package.

5 APPLICATION INFORMATION

5.1 Power Supply

HDG205 should be powered by a single supply voltage on VBAT of 2.85– 4.5V. It generates the digital supply voltage VDD_1.5V with the built in DC-DC converter only requiring an external 3.3uH inductor.

5.1.1 Main supply

The main power is connected to VBAT. The ripple on VBAT should be less than 10mV p-p. External decoupling capacitors should be connected, min 1uF.

The 1.5V is generated by an internal DC-DC converter. The DC-DC converted requires an external 3.3uH inductor between pin 25 and pin 26.

The 1.5V supply can also be fed externally if available in the application. The externally fed 1.5V should be turned off when the HDG205 is in Shutdown mode.

5.2 Clock Signals

The HDG205 requires no external clock signals. It has an internal oscillator with a high precision 40 MHz crystal to generate the required clock signals.

5.3 Shutdown

The SHUTDOWN pin shall be set high during normal operation. Pulling the SHUTDOWN pin low, sets HDG205 in Shutdown mode. This turns OFF most parts of the circuit and minimizes the current consumption. All I/O interface pins are set to predefined states (high, low or high-z) when in Shutdown mode. For minimum power consumption turn external 1.5 V, OFF while the SHUTDOWN pin is low.

To end Shutdown mode set SHUTDOWN pin high and reload FW

5.4 Power save

Power save is an energy saving mode where HDG205 is only listening at regular intervals for the beacons transmitted from an access point and is set in sleep mode in between. During this sleep mode, FW is kept in RAM but all not needed functions are turned off. Since the receive time is very short compared to the listening interval the average current consumption is reduced significantly.
The timing of the listening interval is based on the LFC (32 kHz) clock. The LFC is implemented internally but can also be fed externally. See Low frequency clock, LFC External power enable

5.5 Initialization

At power on and after reset the HDG205 will load firmware and calibrate the radio. The UARTb_SPI signal will be sampled at the end of the initialization period.

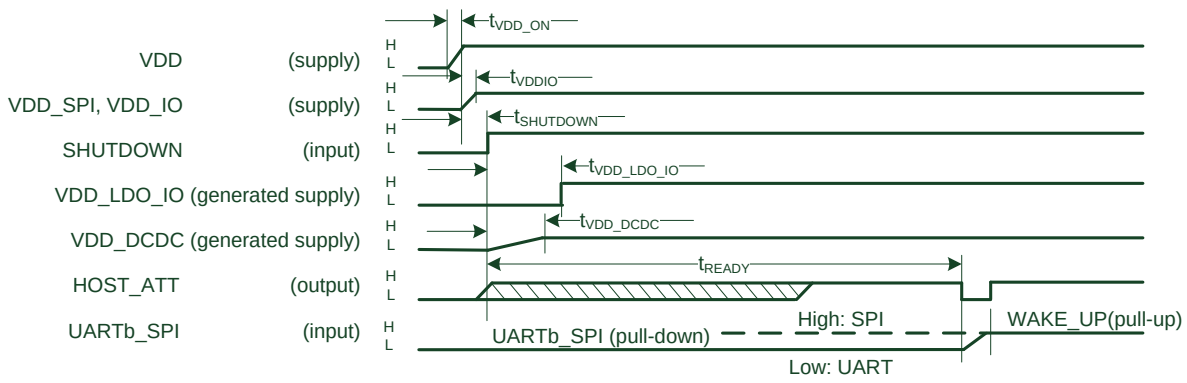

Figure 6: Initialization timing

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VDD rise time	t_{VDD_ON}	2			µs	
VDD_SPI, VDD_IO turn on	t_{VDDIO}	0			µs	
SHUTDOWN release delay	$t_{SHUTDOWN}$	1			ms	
IO supply ramp time	$t_{VDD\_LDO\_IO}$		360		µs	
Digital 1.5V supply ramp time	t_{VDD_DCDC}		150		µs	
SHUTDOWN release to host alert	t_{READY}		4		s	

Table 8: Initialization timing

5.6 Shutdown sequence

The following shutdown procedure shall be used for a shutdown and start up sequence of the HDG205, when a 40MHz crystal is used. FW and optionally the MIB data are reloaded from the host when restarting from SHUTDOWN. Note that all supply voltages are ON during shutdown except DVDD which must be tuned OFF. VPA can optionally be turned OFF. See timing diagram Figure 5-7 and Table 5-9.

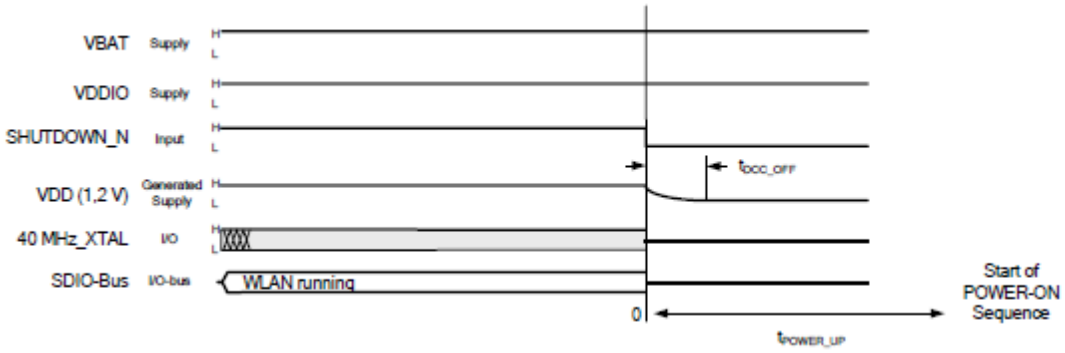

Figure 5-7: Shutdown timing

Parameter S

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DCDC Turn off time	tDCDC_OFF	0	2		ms	
Power up after shutdown	tPOWER_UP	1			ms	

Table 5-9: Shutdown timing

5.7 Power OFF Sequence

All power supplies can be turned OFF at the same time.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VDDIO turn off time	tVDDIO_OFF	0			ms	
VBAT turn off time	tVBAT_OFF	tVDDIO_OFF			ms	

Table 5-10: Power down timing

5.8 Selecting UART or SDIO/SPI as host interface

By setting UARTb_SPI low or high during the initialization the type of host interface can be selected.
If UARTb_SPI is set low UART will be selected as host interface
If UARTb_SPI is set high SDIO/SPI will be selected as host interface.
Note that the UARTb_SPI is sampled every time the HDG205 initializes, at power on and after SHUTDOWN signal are released.
The UARTb_SPI signal has an internal pull-up so if left unconnected SDIO/SPI will be selected as interface.
After initialization the UARTb_SPI pin switch function to WAKE_UP.

5.8.1 Host Interface SDIO/SPI

Default at Power On is SDIO 1-bit mode. The host must send the appropriate command in SDIO 1-bit mode to change to SDIO 4-bit mode or to SDIO SPI-mode.

Host interface mode selection is done on the first host command received after Power ON Reset.

Let host send a valid SDIO 1-bit command, this will set the interface to SDIO/SPI-mode.

All unused interface pins shall be left open.

For timing characteristics and trigger level see Figure 3-3 and Table 3-5 or Figure 3-4 and Table 3-6.

5.8.2 UART host interface

If UARTb_SPI is low during initialization of the HDG205 the UART1_TX and UART1_RX will become the host interface of the HDG205

To communicate with the HDG205 an UART interface is used. The signals “UART1_RTS” and “UART1_CTS” are only active when hardware flow control is enabled by commands from the host.

For UART mode the default setting is 115200 bps, 8 bits, no parity, 1 stop bit.

The HDG205 supports baud rates from 9600 baud up to 4 000 000 baud on the UART interface.

5.8.3 SPI Interface

The SPI interface is only used on board HDG205 to connect to a small EEPROM, that stores individual data (MAC address, calibration data etc.).

5.8.4 Host Wake up

Wake up command via the SDIO interface. This is the normal wake up and is implemented in the FW.

If a dedicated pin is needed as in UART host mode, pin 39 (HOST_WAKEUP) can be used. This requires a dedicated FW. Please contact H&D Wireless for more information.

5.8.5 Real Time Clock I/O (EXT_LFC)

This pin is pre-assigned as Low Frequency Clock (LFC), 32kHz, Real Time Clock input.

If no clock is available on this pin the internal LFC is used. If a clock is available on this pin it can be used as LFC. This pin shall be left open if not used.

5.8.6 Test interface

The pins for JTAG (ICE_TMS, ICE_TDI, ICE_TDO, ICE_TRST and ICE_TCK) is for module production test only. Leave unconnected.

5.9 RF interface

The RF output pin impedance is 50 ohm and shall be connected to an antenna with VSWR much better than 2:1.

5.10 General application information

5.10.1 Design directions

The design using the HDG205 must be performed according to good RF design considerations. All the leads shall be as short as possible between the circuit pins and the external components. Highest priority has the RF-port to antenna strip line.

5.10.2 Soldering

The HDG205 uses a QFN package. The recommended solder profile is pictured in Figure 5-8
Before assembly it is recommended to bake the HDG205 for 5d at 60 °C in Tape&Reel or for 8h at 120 °C with no packaging.

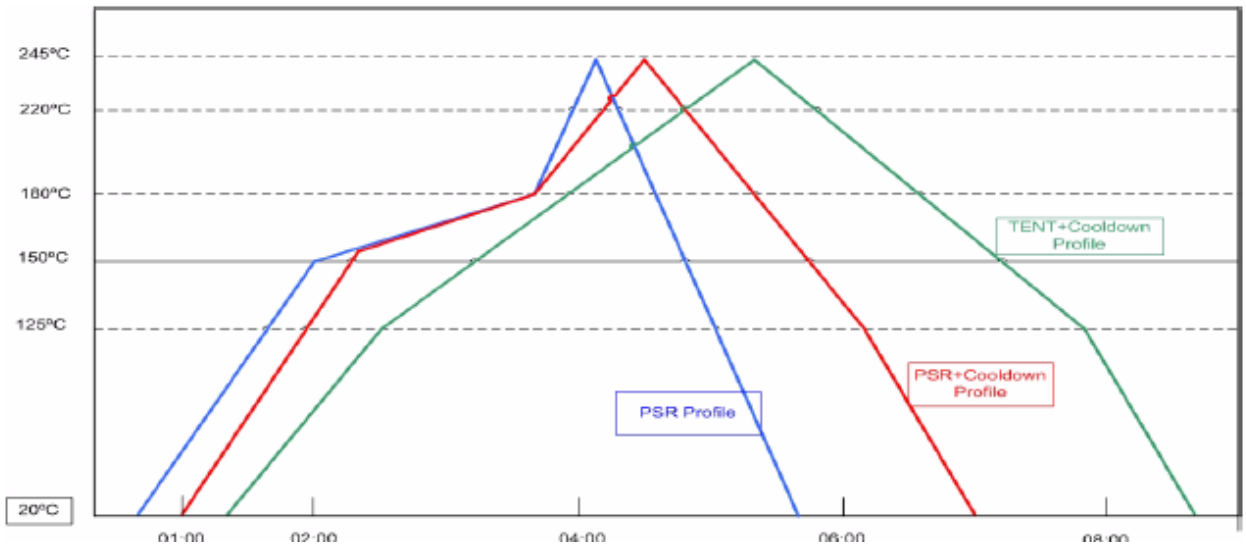

Figure 5-8: Reflow Temperture Profile

Type	Rising Zone	Preheat Zone	Reflow Zone	Peak Zone	Cooldown Zone	Comment
PSR	125ºC-Peak No	150-180ºC 60-120 s	>220ºC 30-60 s	240-255ºC	Peak-125ºC No	O_2< 500ppm
PSR + Cooldown	125ºC-Peak No	150-180ºC 60-120 s	>220ºC 30-60 s	240-255ºC	Peak-125ºC < 1ºC/s	
TENT + cooldown	125-217ºC < 1ºC/s	125-217ºC 150-210 s	>217ºC 60-90 s	240-255ºC	Peak-125ºC < 1ºC/s	

5.10.3 Environmental statement

The HDG205 is designed and manufactured to comply with the RoHS and Green directives.

6 Package Specifications

6.1 Mechanical outline QFN 44 pin

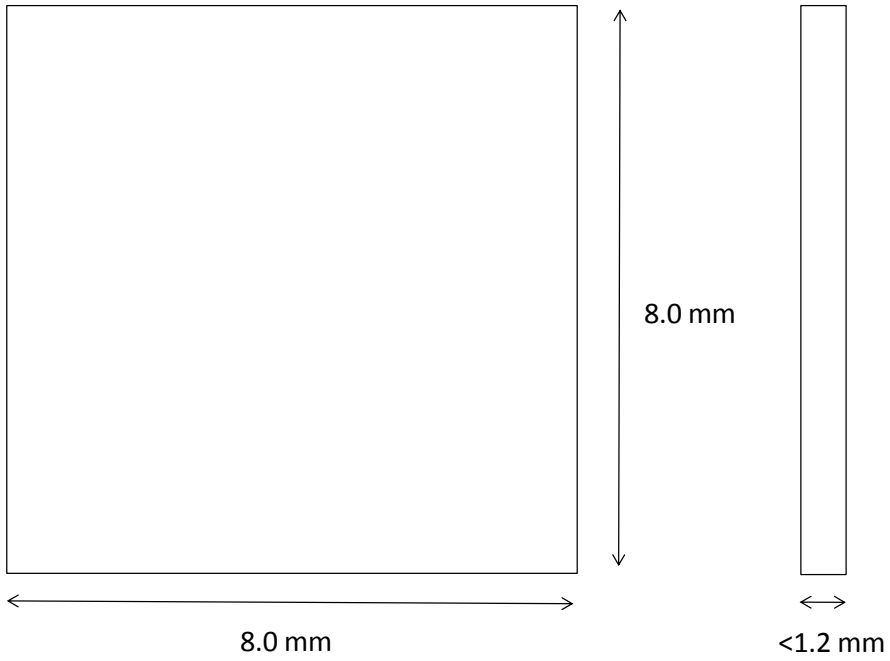

Figure 6-1: Mechanical drawing, 44 pin Quad Flat No-Lead (QFN) package.

Package specifications

6.2 Marking HDG205 QFN

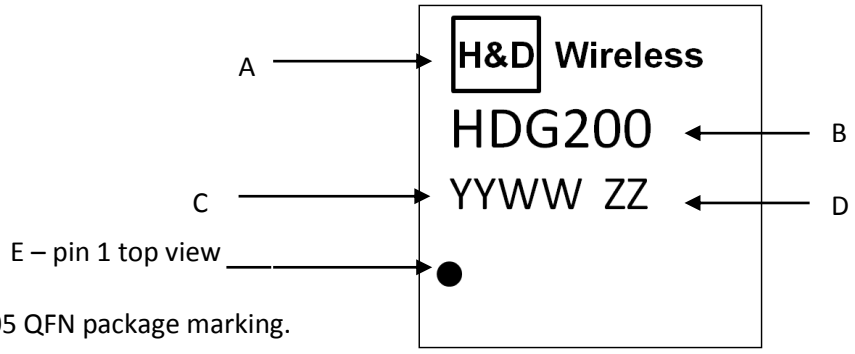

Figure 5-4: HDG205 QFN package marking.

Ref	Marking	Description
A	H&D Wireless	Company Logo
B	HDG205	Product name
C	YYWW	Production date. YY= year, WW=week
D	ZZ	Production lot
E	Square	Defines pin 1 (Top view)

Table 6-1: QFN package marking description

6.3 Package pad dimension

HDG205 pad placement and sizes, top view. Units in mm.

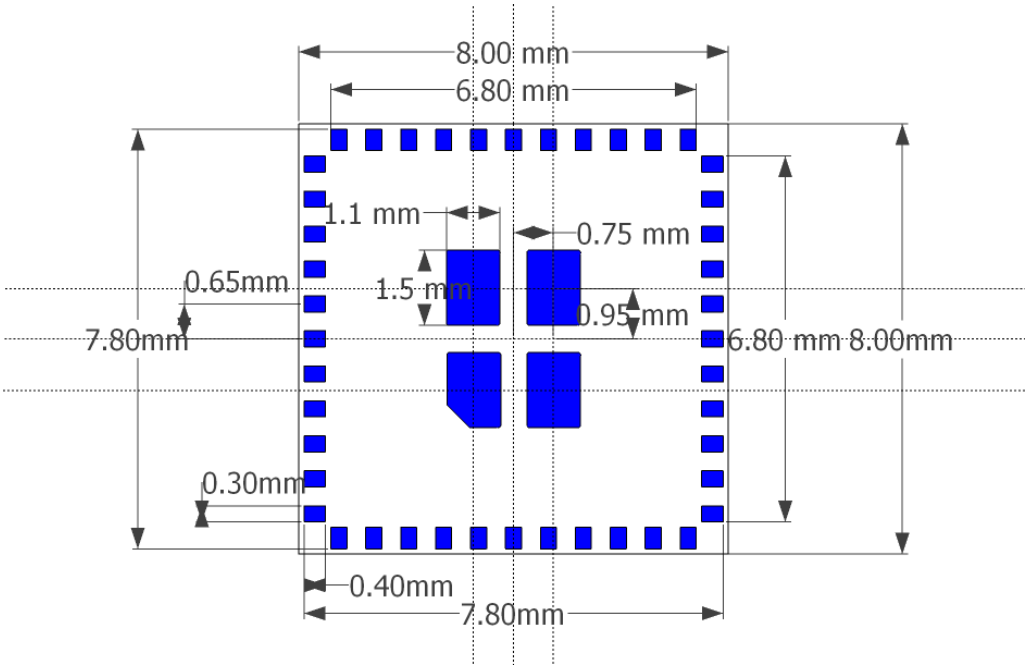

Figure 5.5: HDG205 Pad pattern, top view, units in mm

6.4 Mounting information

Recommended land pattern on the PCB

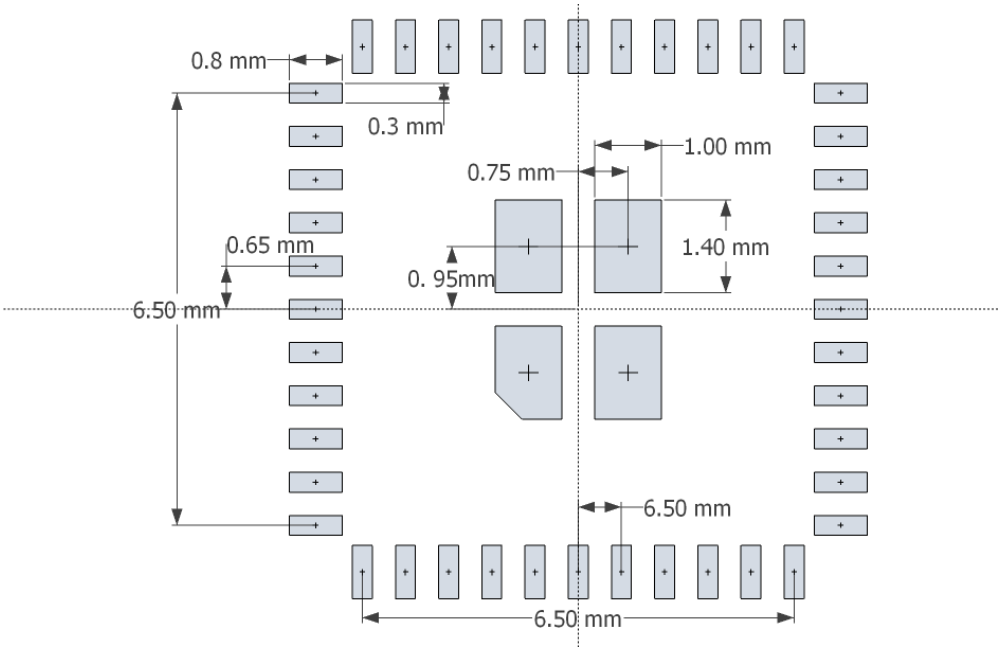

Figure 5.6: Recommended land pattern on the PCB, top view

7 STANDARDS COMPLIANCE

7.1 IEEE/IETF

Standard	Revision	Description
802.11	802.11™ –R2003	WLAN MAC& PHY
802.11b	802.11™ –R2003	High Rate DSSS (5,5/11 Mbit/s)
802.11d	802.11™ –R2003	Operation in different regulatory domains
802.11g	-2003	Extended rate PHY (ERP-PBCC, DSS-OFDM)
802.11i	-2004	Security enhancements
802.11n	2009	WLAN MAC&PHY Amendment 5
802.11r	2008	Amendment 2: Fast Basic Service Set (BSS) Transition
802.11h	1997 edition	Bridge tunneling
RFC1023	Inherent	Frame encapsulation

Table 7.1: applicable IEEE standards

7.2 WiFi

Specification	Description	Revision
Wi-Fi 802.11b with WPA system inter operability test plan for IEEE 802.11b devices	802.11b devices with WPA	2.1
WiFi 802.11g with WPA system inter operability test plan	802.11g devices with WPA	2.0
WMM (including WMM Power Save)		Ver 1.1
WPS (Wireless Protected Setup)		

Table 7.2: Applicable WiFi standards

7.3 Regulatory

Country	Approval authority	Regulatory	Frequency band
USA	FCC	FCCID: XO2HDG200	2.412 GHz -2.462 GHz
Canada	IC	TBA	2.412 GHz -2.462 GHz
Europe	Self Certification	ETSI	2.4 GHz -2.4835 GHz

Table 7.3: Regulatory standards

7.3.1 FCC (United States of America)

This equipment complies with Part 15 of the FCC rules and regulations.
To fulfill FCC Certification requirements, an OEM manufacturer must If the HDG205 module are incorporated into a product, ensure compliance of the final end-user product.

The modular transmitter must be labeled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module.

WARNING: The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment.

IMPORTANT: This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19).

The internal / external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance. This device is approved as a mobile device with respect to RF exposure compliance, and may only be marketed to OEM installers. Use in portable exposure conditions (FCC 2.1093) requires separate equipment authorization.

IMPORTANT: Modifications not expressly approved by this company could void the user's uthority to operate this equipment (FCC section 15.21).

IMPORTANT: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense (FCC section 15.105).

7.3.2 IC (Canada)

Equipment is subject to certification under the applicable RSSs, shall be permanently labeled on each item, or as an inseparable combination. To fulfill RSS Certification requirements, an OEM manufacturer must if the HDG205 module is incorporated into a product ensure compliance of the final end-user product**.**

IMPORTANT: This equipment for which a certificate has been issued is not considered certified if it is not properly labeled. The information on the Canadian label can be combined with the manufacturer's other labeling requirements

IMPORTANT: Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT: To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

IMPORTANT: The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population. Consult Safety Code 6, obtainable from Health Canada's website www.hc-sc.gc.ca/rpb.

7.3.3 ETSI (Europe)

The HDG205 module has been certified for use in European union countries according to ETSI EN 300 328 (Electromagnetic compatibility and Radio spectrum matters for equipment operating in the 2,4 GHz ISM band using spread spectrum modulation techniques). This standard is harmonized within the European Union and covering essential requirements under article 3.2 of the R&TTE-directive.

If the HDG205 module are incorporated into a product, the manufacturer must ensure compliance of the final end-user product to the European harmonized EMC and low voltage/safety standards. A declaration of conformity must be issued for the product including compliance references to these standards. Underlying the declaration of conformity a technical construction file (TCF), including all relevant test reports and technical documentation, must be issued and kept on file as described in Annex II of the R&TTE-directive.

Furthermore, the manufacturer must maintain a copy of the HDG205 module documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a complete re-test must be made in order to comply with all relevant standards as basis for CE-marking. A submission to notified body must be used only if deviations from standards have been found or if non-harmonized standards have been used.

8 SALES OFFICES

Global Sales Office Sweden

H&D Wireless AB
H&D Wireless AB
Norgegatan 1
164 32 Kista
Sweden

E-mail: info@hd-wireless.se
Support: support@hd-wireless.se
Home page: www.hd-wireless.se

Local sales offices and distributors see **www.hd-wireless.se**

9 Reference designs

9.1 Reference design using HDG205

This document describes how to use the HDG205 SIP component in a customer application.
See www.hd-wireless.se for the complete list of reference designs and other support documents.